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EXAMINER	
SAVLA, ARPAN P	

ART UNIT	PAPER NUMBER
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,083	MANDLER, ALBERTO RODRIGO	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/23/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. 10/791,083 has a total of 56 claims pending in the application, there are 4 independent claims and 52 dependent claims, all of which are ready for examination by Examiner.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

1. Applicant's oath/declaration has been reviewed by Examiner and is found to conform to the requirements prescribed in 37 CFR 1.63.

INFORMATION CONCERNING DRAWINGS

Drawings

2. Applicant's drawings submitted March 2, 2004 are acceptable for examination purposes.

ACKNOWLEDGMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

3. As required by MPEP § 609(c), Applicant's submission of Information Disclosure Statement dated January 23, 2006 is acknowledged by Examiner and cited references have been considered in the examination of the claims now pending. As required by MPEP § 609 c(2), a copy of the PTOL-1449 initialed and dated by Examiner is attached to the instant office action.

OBJECTIONS

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested: "Conditionally Accessible Cache Memory Based Upon Fulfillment Of A Locking Condition."

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 12, 14, and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. **As per claim 12**, the claim recites the limitation "said memory access command" on pg. 20, lines 16-17. There is insufficient antecedent basis for this limitation in the claim. Applicant may consider amending the claim to read "said memory access instruction."

8. **As per claim 14**, the claim recites the limitation "said memory access command" on pg. 20, line 24. There is insufficient antecedent basis for this limitation in the claim. Applicant may consider amending the claim to read "a memory access command."

9. **As per claim 15**, the claim recites the limitation "said accessor" on pg. 20, line 28. There is insufficient antecedent basis for this limitation in the claim. Applicant may consider amending the claim to read "a accessor" or making claim 15 dependent on claim 2.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1-17, 20-24, 26-33, 35-48, and 51-56 are rejected under 35 U.S.C. 102(b) as being anticipated by Maheshwari (U.S. Patent 5,974,508).

12. **As per claim 1**, Maheshwari discloses a cache memory having a conditional access mechanism operated by a locking condition, for conditionally locking said cache memory (col. 4, lines 13-15; Fig. 1, elements 150 and 151).

13. **As per claims 2, 27, and 36**, Maheshwari discloses said conditional access mechanism comprises:

a condition checker, for determining fulfillment of said locking condition (col. 7, lines 20-22; Fig. 7, element 701); *It should be noted "lock signal producer" is analogous to "condition checker."*

a hit determiner, for giving hit and miss indications for data stored in said cache memory (col. 2, lines 29-30; col. 6, lines 46-60; Fig. 6)

and a cache accessor, for conditionally implementing a cache memory access in accordance with the fulfillment of said locking condition (col. 2, lines 65-67; col. 7, lines 22-25; Fig. 1, element 120). *It should be noted that "bus interface unit (BIU)" is analogous to "cache accessor."*

14. **As per claim 3**, Maheshwari discloses said conditional implementing comprises accessing said cache memory with cached data locked if said locking condition is fulfilled (col. 7, lines 15-19). *It should be noted that the caches are being accessed while the caches are locked (i.e. the locking condition is fulfilled).*

15. **As per claims 4, 28, and 37**, Maheshwari discloses said conditional access mechanism is operable to prevent replacement of data stored in a section of a conditionally locked cache memory (col. 4, lines 36-38).

16. **As per claims 5, 29, and 38**, Maheshwari discloses said conditional access mechanism is operable to update data stored in a section of a conditionally locked cache memory (col. 4, lines 42-44).

17. **As per claims 6, 30, and 39**, Maheshwari discloses said conditional access mechanism is operable to prevent reallocation of a section of a conditionally locked cache memory (col. 7, lines 10-11).

18. **As per claims 7, 31, and 40**, Maheshwari discloses said conditional access mechanism is operable to access a section of a conditionally unlocked cache memory, in accordance with a corresponding lock bit (col. 4, lines 16-18; col. 5, lines 4-7). *It*

should be noted that "request" is analogous to "access" and a cache in "normal mode" is analogous to a "conditionally unlocked cache memory." It should also be noted that the entry lock bits determines whether the cached is in one of the locked modes or conversely operating in normal mode.

19. **As per claim 8**, Maheshwari discloses a condition definer, for holding a definition of said locking condition (col. 7, lines 33-36 and 49-51; Fig. 4b, element 401; Fig. 4c, element 402). *It should be noted that the "cache/BIU register" and the "lock control register" comprise the "condition definer." It should also be noted that "global instruction cache lock bit", "global date cache lock bit", "data cache entry auto-lock bit", and "instruction cache auto-lock bit" comprise the "definition of the locking condition."*

20. **As per claim 9**, Maheshwari discloses said definition is updateable during operation (col. 7, lines 37-43; col. 8, lines 8-22; Fig. 4b, elements 410 ands 414; Fig. 4c, elements 420 and 422). *It should be noted that the setting and clearing of these various bits during operation indicates they are updateable.*

21. **As per claim 10**, Maheshwari discloses said definition comprises a condition type and parameters associated with said type (col. 5, lines 42-52 and 55-64; col. 7, lines 52-65). *It should be noted that "global locking mode" or "local locking mode" is analogous to "condition type" and that the high or low level of the various lock bits is analogous to "parameters associated with the condition type."*

22. **As per claims 11 and 44**, Maheshwari discloses said locking condition is fulfilled if a currently accessed main memory location comprises a main memory location specified by said locking condition (col. 4, lines 7-9; col. 5, lines 10-13; Fig. 5). *It should*

be noted that "memory-mapped address" refers to a memory location in "external memory 125" which is analogous to "main memory."

23. **As per claims 12 and 45**, Maheshwari discloses each main memory access instruction has a type, and wherein said locking condition is fulfilled if a type of said memory access command comprises a command type specified by said locking condition (col. 5, lines 25-29). *It should be noted that "write" is the "type of memory access instruction."*

24. **As per claim 13**, Maheshwari discloses said cache memory comprises a conditional locking indicator, and wherein said locking condition is fulfilled if said conditional locking indicator is set (col. 5, lines 4-5; col. 8, lines 12-13; Fig. 3, element 305). *It should be noted that "cache entry lock bit" is analogous to "conditional locking indicator."*

25. **As per claim 14**, Maheshwari discloses said memory access command comprises a conditional locking parameter, for turning on conditional locking during the execution of said command (col. 5, lines 25-29). *It should be noted that "the value of the entry lock bit (by either setting or clearing it)" is analogous to a "conditional locking parameter."*

26. **As per claim 15**, Maheshwari discloses said accessor is operable to turn conditional accessing on and off in accordance with a predetermined memory access command (col. 5, lines 25-29; col. 7, lines 20-25; Fig. 7, elements 701, 702, and 703).

27. **As per claim 16**, Maheshwari discloses said cache memory is for caching data of an associated main memory (col. 3, lines 30-34; Fig. 1, elements 125 and 151). *It should be noted that "external memory" is analogous to "main memory."*

28. **As per claim 17**, Maheshwari discloses said cache memory is further associated with a processor operable to access said associated main memory via said cache memory (col. 3, lines 30-36; Fig. 1, elements 100, 125, and 151). *It should be noted that "CPU" is analogous to "processor."*

29. **As per claim 20**, Maheshwari discloses said conditional access mechanism further comprises a cache invalidator, for invalidating data in specified cache memory sections (col. 4, lines 51-56; col. 7, lines 37-39; col. 6, line 40; Fig. 3, element 302; Table 1). *It should be noted that the Integer Unit (IU) issues an Address Space Identifier (ASI) which in turn controls the valid bit of the instruction and data cache tags. Therefore, the "IU" is analogous to the "cache invalidator."*

30. **As per claim 21**, Maheshwari discloses said cache memory comprises an associative memory (col. 4, lines 1-2).

31. **As per claim 22**, Maheshwari discloses a cache memory section comprises a cache memory way (col. 4, lines 2-3; Fig. 2, elements 203 and 204). *It should be noted that "bank" is analogous to "way."*

32. **As per claim 23**, Maheshwari discloses a said cache memory comprises an n-way set associative memory (col. 4, lines 1-2). *It should be noted that n=2.*

33. **As per claim 24**, Maheshwari discloses a cache memory section comprises an index of said n-way set associative cache memory (col. 4, lines 4-6). *It should be noted that "address bits <9:4>" is analogous to "index."*

34. **As per claim 26**, Maheshwari discloses a memory system comprising:

a main memory (col. 2, lines 50-51; Fig. 1, element 125);

and a cache memory associated with said main memory, for caching data of said main memory, and having a conditional access mechanism configurable with a locking condition, for conditionally locking said cache memory (col. 3, lines 30-34; col. 4, lines 13-15; Fig. 1, elements 150 and 151).

35. **As per claim 32 and 41**, Maheshwari discloses said locking condition is conditional upon at least one of the following group: a main memory address, a type of a memory access command, a processor, a processor type, and a locking indicator (col. 5, lines 4-5; Fig. 3, element 305). *It should be noted that "cache entry lock bit" is analogous to "locking indicator."*

36. **As per claim 33**, Maheshwari discloses a memory system associated with a processor operable to access said main memory via said cache memory (col. 3, lines 30-36; Fig. 1, elements 100, 125, 150, and 151).

37. **As per claim 35**, Maheshwari discloses a processing system comprising:

a main memory (col. 2, lines 50-51; Fig. 1, element 125);

a cache memory associated with said main memory, for caching data of said main memory, and having a conditional access mechanism configurable with a locking

condition, for conditionally locking said cache memory (col. 3, lines 30-34; col. 4, lines 13-15; Fig. 1, elements 150 and 151);

and a processor associated with said cache memory, operable to access said main memory via said cache memory (col. 3, lines 30-36; Fig. 1, elements 100, 125, 150, and 151).

38. **As per claim 42**, Maheshwari discloses a method for conditionally locking a cache memory, said cache memory comprising multiple sections for caching the data of an associated main memory (col. 3, lines 30-34; col. 4, lines 1-6 and 13-15; Fig. 1, elements 150 and 151), comprising:

specifying a locking condition (col. 5, lines 4-5; Fig. 3, element 305);

and performing conditional accesses to said cache memory in accordance with a main memory access command and the fulfillment of said locking condition (col. 5, lines 25-29).

39. **As per claim 43**, Maheshwari discloses said cache memory comprises lock bits corresponding to said sections (col. 5, lines 4-5; Fig. 3, element 305), and wherein said performing comprises:

if said locking condition is fulfilled, accessing said cache memory with cached data locked (col. 7, lines 15-19); *It should be noted that the caches are being accessed while the caches are locked (i.e. the locking condition is fulfilled).*

and if said locking condition is not fulfilled, accessing said cache memory in accordance with said lock bits (col. 4, lines 16-18). *It should be noted "normal mode" is analogous to "locking condition is not fulfilled."*

40. **As per claim 46**, Maheshwari discloses said locking condition is fulfilled if a conditional locking indicator is set (col. 5, lines 4-5; col. 8, lines 12-13; Fig. 3, element 305).

41. **As per claim 47**, Maheshwari discloses said main memory access command comprises a conditional locking parameter, and wherein said locking condition is fulfilled if said conditional locking parameter is set (col. 5, lines 4-5 and 25-29; col. 8, lines 12-13; Fig. 3, element 305).

42. **As per claim 48**, Maheshwari discloses said main memory access commands originate from an associated processor (col. 2, lines 51-54; Fig. 1, element 100).

43. **As per claim 51**, Maheshwari discloses said conditional accessing comprises preventing reallocation of a section of a conditionally locked cache memory (col. 7, lines 10-11).

44. **As per claim 52**, Maheshwari discloses said cache memory comprises lock bits corresponding to said sections, and wherein said conditional accessing comprises accessing a cache memory section in accordance with a corresponding lock bit, if said locking condition is not fulfilled (col. 5, lines 4-5; col. 4, lines 16-18; Fig. 3, element 305).

45. **As per claim 53**, Maheshwari discloses said cache memory comprises lock bits corresponding to said sections (col. 5, lines 4-5; Fig. 3, element 305), and wherein said conditional accessing comprises:

if a current cache access comprises a read access, performing a cache read operation to said cache memory (col. 6, lines 51-53);

if a current cache access comprises a write access, performing:

determining if said locking condition is fulfilled (col. 7, lines 20-22; Fig. 7, element 701);

if said locking condition is fulfilled:

if a cache hit is obtained for a main memory location associated with said current cache access, performing a cache write operation to update cached data (col. 4, lines 42-44; col. 5, lines 46-48); and if a cache miss is obtained for said location, performing a cache write operation with cached data locked against replacement (col. 7, lines 15-19); *It should be noted that "read miss" is analogous to "cache miss."*

and if said locking condition is not fulfilled, performing a cache write operation in accordance with said lock bits (col. 4, lines 16-18 and 21-24).

46. **As per claim 54**, Maheshwari discloses specifying a parameter of said locking condition (col. 5, lines 25-29). *It should be noted that "the value of the entry lock bit (by either setting or clearing it)" is analogous to a "parameter of the locking condition."*

47. **As per claim 55**, Maheshwari discloses updating said locking condition (col. 5, lines 25-29). *It should be noted that the "write instruction" "updates the lock bits."*

48. **As per claim 56**, Maheshwari discloses invalidating data cached in said cache memory (col. 4, lines 51-56; col. 7, lines 37-39).

Claim Rejections - 35 USC § 103

49. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

50. Claims 18-19 and 49-50 are rejected under 35 U.S.C. 103(a) as being obvious over Maheshwari in view of Vartti (U.S. Patent Application Publication 2002/0174305).

51. **As per claim 18**, Maheshwari discloses all the limitations of claim 18 except said locking condition is fulfilled if said processor comprises a processor specified by said locking condition.

Vartti discloses said locking condition is fulfilled if said processor comprises a processor specified by said locking condition (paragraph 0055, lines 18-21 and 25-26; paragraph 0056, lines 1-4). *It should be noted that the "lock request" and "lock grant" comprise the "locking condition." It should also be noted that when a requesting processor sends out a "lock request" to the "SC" it specifies itself (i.e. requesting processor) as the processor wanting ownership.*

Maheshwari and Vartti are analogous art because they are from the same field of endeavor, that being cache locking.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Vartti's lock request specifying a processor wanting ownership within Maheshwari's cache locking system.

The motivation for doing so would have been to provide a storage lock independent of the need for specific hardware in the storage or storage control, and therefore allowing generic memory controllers to be used in the processing environment, therefore, providing a more efficient and effective system (Vartti, paragraph 0008, lines 11-15 and 4-5).

Therefore, it would have been obvious to combine Maheshwari and Vartti for the benefit of obtaining the invention as specified in claim 18.

52. **As per claim 19**, Vartti discloses a processor has a type, and wherein said locking condition is fulfilled if a type of said processor comprises a processor type specified by said locking condition (paragraph 0055, lines 18-21 and 25-26; paragraph 0056, lines 1-4). *It should be noted that in a multi-processor system such as Vartti's it is inherently required each processor have some sort of unique identification (ID) in order to distinguish the processors from each other. This unique ID would be analogous to each processor having a "type." Therefore, when a requesting processor sends out a "lock request" to the "SC" it specifies itself by its ID (i.e. type) as the processor wanting ownership.*

53. **As per claim 49**, Vartti discloses said locking condition is fulfilled if said associated processor comprises a processor specified by said locking condition (paragraph 0055, lines 18-21 and 25-26; paragraph 0056, lines 1-4). *See citation note for claim 18 above.*

54. **As per claim 50**, Vartti discloses said locking condition is fulfilled if a type of said associated processor comprises a processor type specified by said locking condition

(paragraph 0055, lines 18-21 and 25-26; paragraph 0056, lines 1-4). *See citation note for claim 19 above.*

55. Claim 25 is rejected under 35 U.S.C. 103(a) as being obvious over Maheshwari in view of John L. Hennessy and David A. Patterson, "Computer Organization and Design, The Hardware/Software Interface, Second Edition", hereafter "Patterson."

56. Maheshwari discloses all the limitations of claim 25 except said cache memory comprises a direct-mapped memory.

Patterson discloses a direct mapped cache (pg. 546, paragraph 1, lines 5-8).

Maheshwari and Patterson are analogous art because they are from the same field of endeavor, that being cache memory.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Patterson's direct mapped cache as the mapping structure for Maheshwari's cache memories.

The motivation for doing so would have been to exploit the simplicity of direct mapping because if the number of entries in the cache is a power of two, then modulo can be computed simply by using only the low-order $\log_2$ (cache size in blocks) bits of the address; hence the cache may be accessed directly with the low-order bits (Patterson, pg. 546, paragraph 2, lines 1-4).

Therefore, it would have been obvious to combine Maheshwari and Patterson for the benefit of obtaining the invention as specified in claim 25.

57. Claim 34 is rejected under 35 U.S.C. 103(a) as being obvious over Maheshwari in view of BUG Computer Club Home Page entitled, "EDRAM (Embedded DRAM)", hereafter "BUG."

58. Maheshwari discloses all the limitations of claim 25 except said main memory comprises an embedded dynamic random access memory (EDRAM).

BUG discloses an EDRAM (paragraph 1, lines 1-3).

Maheshwari and BUG are analogous art because they are from the same field of endeavor, that being computer memory.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement BUG's EDRAM as the memory structure for Maheshwari's external memory.

The motivation for doing so would have been to include a small amount of SRAM inside a larger amount of DRAM so that memory accesses will be to the faster SRAM (BUG, paragraph 1, lines 2-4).

Therefore, it would have been obvious to combine Maheshwari and BUG for the benefit of obtaining the invention as specified in claim 34.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1-56** have received a first action on the merits and are subject of a first action non-final.

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

1. U.S. Patent 5,249,286 discloses selectively locking memory locations within a microprocessor's on-chip cache.

2. U.S. Patent 6,141,734 discloses a technique for implementing load-locked and store-conditional instruction primitives by using a local cache for information about exclusive ownership.

3. U.S. Patent 6,629,212 discloses high speed lock acquisition mechanism with time parameterized cache coherency states.

4. U.S. Patent 6,671,779 discloses management of caches of the type where data in the cache may be designated as locked to prevent that data from being overwritten.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Arpan Savla
Assistant Examiner
Art Unit 2185
March 24, 2006

DONALD SPARKS
SUPERVISORY PATENT EXAMINER